Final Report
for
Study of Cold-Substrate Deposition of Thin Film Passive Elements

NAS 12-109

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National Aeronautics and Space Administration

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ABSTRACT

This program is a feasibility study of the fabrication of thin film passive elements by the "Cold Substrate Deposition Process". The thin film passive elements referred to are resistors and capacitors. Cold substrate deposition is a unique film forming process developed by the Librascope Group of General Precision, Inc. A number of benefits are inherent in this process. Two of particular importance to this program are (1) the ability to form a very thin film of high integrity, and (2) the tenacious bonding that is obtained between deposited film and substrate, achievable with a wide variety of materials systems without increasing the temperature of the bulk substrate above room ambient.

The goals of this program are to demonstrate that the process can be used to advantage to form arrays of resistors ranging from 10^2 to 10^5 ohms per square, and arrays of capacitors of 60,000 pico-farads per square inch. Such devices were successfully prepared, and have electrical properties which demonstrate the potential advantages of the process in this area of application.

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1.0 INTRODUCTION AND SUMMARY

The objective of the present contract is to demonstrate the feasibility of forming high performance thin film passive elements by cold substrate deposition. The elements of specific interest are resistors and capacitors. The design goals for the element characteristics were purposely set to advance the state of technology established. The results of the studies and experiments conclusively indicate that the Cold Substrate Deposition Process employed can produce resistors and capacitors having advanced characteristics. The important aspect of this process is the uniformity with which the necessary materials can be deposited to attain thinner continuous film. In the case of the resistor, this leads to higher resistance values per square without significant penalties in performance characteristics, in the case of capacitors the process gives high specific capacitance, consistent with satisfactory voltage breakdown and dissipation characteristics.

For resistors, eight design goal criteria were considered as objectives for each of four resistance ranges: 100, 1,000, 10,000, and 100,000 ohms per square. Each of the design goals was met by devices of both 100 and 1,000 ohms per square. Devices of 10,000 ohms per square met five of the eight design goals and approached meeting a sixth. Devices of 100,000 ohms per square met five design goals. Substrate numbers for specimens meeting goals are tabulated in Appendix II.

The results of the program definitely demonstrate that resistors of sheet resistance up to 1,000 ohms per square and having completely satisfactory properties, can be fabricated by cold substrate deposition. Resistors of 10,000 and 100,000 ohms per square can be presently fabricated by this technology, if some moderate tradeoffs of characteristics are accepted. There is a definite indication that eventually even these tradeoffs will be unnecessary.

Further results of the program show that capacitors up to 60,000 pf/in^2 with desirable voltage and temperature characteristics can be prepared. There were eight design goals set for capacitors; four of these were met

without qualification. Three more were met conditionally (by less stringent tests which are commonly accepted). The final design goal for capacitor (stability under a high temperature environment) was approached, but not met. All devices showed a change of capacitance in excess of the desired range, but this change was consistent on a percentage basis for all devices. It is striking to note that the Cold Substrate Deposition Process permitted the fabrication of capacitors with values in excess of 2,000,000 pf/in^2 using a silicon monoxide dielectric.

This report includes an outline of the overall fabrication techniques used, the equipment and procedures used for testing, tables of raw test data, and evaluation of the results of the program, and recommended steps to further exploit this process, including the development of commercial production techniques. Data and evaluations of the two types of passive elements are presented separately. A separate analysis section contains information of interest with regard to composition, morphology, and geometry of resistive and dielectric films and their relationships to electrical properties regardless of method of fabrication.

The design goals for the study are listed in Appendix I. This is followed by a copy of a communication, titled, "Technique for Photomasking on Light Scattering Substrate Materials", which is being submitted to the Review of Scientific Instruments for publication.

2.0 RESISTORS

This section describes, in chronological sequence, the steps taken in the fabrication, by cold substrate deposition, of multiple thin film resistors on a single substrate in five ranges of resistance. The materials chosen and the type equipment employed for fabrication, control and test are considered in detail. Problems encountered and how they were resolved or what remains to be done are discussed. All significant raw data are tabulated. Finally, an evaluation is presented of the results achieved, as verified by the test data, versus the design goals, as summarized in Appendix I.

At the beginning of the program, the first problem which was encountered and solved, was that of using rejection masks on light scattering substrates. It was found that exceedingly poor image resolution resulted when using rejection masking techniques on glazed alumina substrate. This was determined to be a consequence of internal backscattering of light. The solution was the use of a thin layer of silicon monoxide applied directly on the glazed surface of the substrate. This material absorbs strongly in the wavelengths to which the photoresist is sensitive, thereby eliminating the backscattering. Any light which could degrade the image would have to survive a double pass through this layer. The layer was just thick enough to preclude this degradation with certainty.

The second problem area encountered was the drift of sheet resistance of resistors upon venting the vacuum chamber to the atmosphere. This was solved by depositing a layer of silicon monoxide directly on the resistive material immediately after its deposition. This provides a dense coating of a suboxide which will not readily release its oxygen to the resistive metal film. The films used for this coating were generally of the order of 5,000 angstroms in thickness, though it appeared that 1,000 angstroms may have been sufficient. The initial variation of uncoated films was as great as 10 percent upon exposure to atmosphere. The coating permitted fabrication of samples such as 66A14 and 66A5 which contained specific devices whose variations were within the experimental measurement error during the characterization for all design goals, including the 100 hour

test for stability at 145° C.

The next area requiring work was that of obtaining uniformity over a large area. The cold substrate deposition process follows the well known cosine squared law of distribution. This means that the thickness of the deposit reduces as the square of the cosine of the angle of incidence. In order to reduce this effect, a rotating sector shutter was introduced. With this shutter in use, geometrically dependent resistance variations dropped to less than one percent. The first sample run using the combination of sector shutter and screen mesh was 66A29 with a spread of ± 0.37% from the median value. Wide spreads in runs after this time are due to factors other than simple geometry, specifically, variations in chamber parameters related to the Cold Substrate Deposition Process.

2.1 FABRICATION PROCEDURES

The fabrication procedures employed during the course of the program are described in this section. These have been found to work well as laboratory processes, but would undoubtedly require modification to some extent for pilot production quantities.

Resistor fabrication consists of the following steps: substrate cleaning, SiO undercoat deposition, conductor layer deposition, conductor pattern definition (using photoresist and chemical etching), resistor definition (application of a photoresist rejection mask), resistor layer deposition (immediately followed by a SiO protective overcoat), stripping (removal, via organic solvents, of the rejection mask together with the corresponding portion of the resistor layer) and trimming (to achieve precision resistor values).

All resistor geometries were 3 mm X 3 mm, with four such units per substrate. A typical resistor substrate is shown in Figure 1. The resistor depositions were performed in a vacuum station containing an electron beam evaporant source with multiple crucibles. This station and other equipment employed are described in detail in Section 2.2.

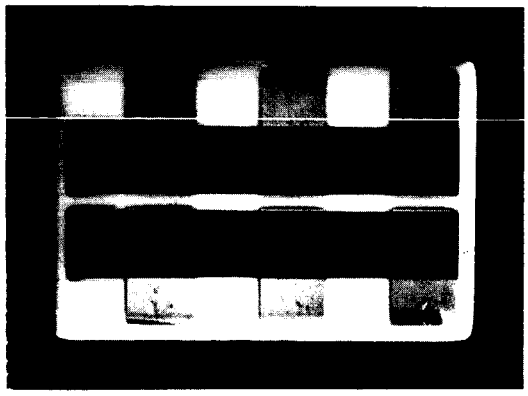

Figure 1. Resistor Substrate

Four Tophet-C Resistors (3mm × 3mm)
on Glazed Alumina Substrate (1/2" x 3/4").

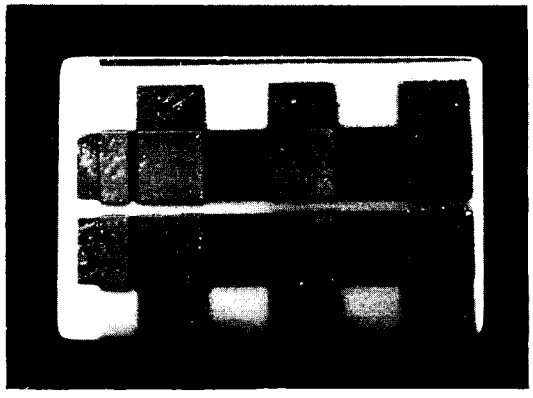

Figure 2. Capacitor Substrate

Six Si O Capacitors (3mm × 3mm)
on Glazed Alumina Substrate (1/2" x 3/4")

2.1.1 Conductor Deposition

The substrates are given a detergent rinse, and are scrubbed with a foam plastic towel to remove loose glaze particles. They are then washed in distilled water, and given electronic-grade solvent rinses. The final drying is by a blast of dry gas to squeegee off the solvent. The system is loaded with a charge of SiO (vacuum outgassed, Linde select grade, + 10 mesh). The substrates are mounted on the work holder, the chamber is closed, and pumped down. The SiO undercoat is deposited and the system is vented. The substrate holder with substrates is removed and temporarily stored in a dust-free environment. The system is then loaded with either titanium-copper-nickel, or titanium-nickel, depending on the conductor resistivity needed. Vacuum outgassed boules are used. Each metal charge is separate, and each is placed in a separate crucible. The substrate holder is replaced and the system is pumped down. The metal layers are then deposited sequentially. The titanium layer is very thin, usual deposition parameters being 15 seconds at 1000 watts power for the electron beam unit. The copper and nickel layers are much thicker, and are normally run for 5 to 15 minutes at 1750 to 2000 watts beam power (depending on the required properties of the conductors). The system is then vented and the substrates are removed for pattern definition.

2.1.2 Conductor Definition

The substrates are transferred by the use of tweezers and other mechanical handling devices from bell jar to microscope where the coatings are examined. They are then moved to a whirling table, coated with 60% KTFR (Kodak Thin Film Resist), and spun at 6,000 RPM. This coating is air dried for 20 minutes and prebaked for 10 minutes at 80°C. Each substrate is then placed on a K & S micropositioner for pattern alignment and exposure. A two second exposure with a Leitz 200 watt U. V. source is used. The resist is then spray developed. The patterns are examined under a low power microscope (selected samples are also examined at 600 power. The patterns are then postbaked at 110°C prior to etching.

The copper and nickel layers are etched with ferric chloride. The titanium flash must be removed with 2% hydrofluoric acid. This etch step is quite critical. Too light an etch will leave a conductive film between electrodes; too deep an etch will undercut the electrodes. A combination of time, visual observation, and electrical check is used. A definite color change can be detected as the etching nears completion. When etching is completed, the photoresist is removed, and the substrates are cleaned for the next operation.

2.1.3 Resistor Definition

The resistor areas are defined by means of rejection masking. Rejection masking is a process in which a removable coating of photoresist is placed on the substrate. The photoresist is exposed through the appropriate photographic negative. This provides a photoresist coating on all areas of the substrate which are not resistor areas. The resistor layer deposition is then performed (as described in Section 2.1.4), and the removable coating is stripped, (see Section 2.1.5), leaving behind a sharply defined resistor pattern. The rejection mask material used is 60% KTFR. The procedure employed is identical to the photresist procedure described in Section 2.1.2, with one exception; a one-second exposure is used rather than a two-second exposure. The image on the substrate is examined under low power and at 600 power prior to a postbake.

2.1.4 Resistor Deposition

One or more substrates and a monitor substrate are mounted on the substrate holder. A freshly measured and coiled charge of Tophet-C wire (composition and source given in Section 2.2.1), is placed in one crucible. A second crucible is loaded with a charge of SiO as described in Section 2.1.1. The system is then pumped down. The Tophet-C is melted and vacuum outgassed for a predetermined time (shutter closed). The crucible is permitted to cool and the system is then purged with argon. The Tophet-C is remelted, and the shutter is opened until the correct reading is obtained on the monitor. The shutter is closed, the melt cooled, and

the SiO is immediately evaporated to cover the resistor. The system is vented and the substrates are removed.

2.1.5 Stripping

The rejection mask is now removed by soaking in a stripping solution (consisting of equal volumes of dichloroethane, trichloroethane, and toluene) and applying a light brushing. This particular solution is used because some of the commercial strippers contain materials which would etch the conductor pattern. The resistor sample is cleaned and is then ready for testing.

2.1.6 Trimming

The method used on this contract for trimming resistors was scribing by a microprobe. The sample being trimmed for adjustment of its resistance was continously monitored with a resistance bridge during the scribing.

2.2 EQUIPMENT AND MATERIALS FOR FABRICATION

This section lists the materials and the equipment used for resistor fabrication and gives some further indications as to their use and/or features.

2.2.1 Materials

All resistors for this program were prepared on American Lava AT-60400-M substrates. These are 1/2 inch by 3/4 inch by 0.030 inch thick. The base is 0.025 inch thick ALSIMAG 614 with a 0.005 inch coating of glaze 743. The glaze 743 is basically a lead boro-silicate glass with an alkali content of about 3%. In use, this is covered by a 1/2 to 1 micron layer of silicon monoxide. The form used is Linde select grade, vacuum outgassed, +10 mesh. The resistor element itself is Tophet-C (which is a 28% iron, 50% nickel, 12% chromium alloy obtained from Wilbur B. Driver Company). The wire used is size 20, with a resistance of 0.673 ohms/ft. The titanium, copper, and nickel presently being used are commercially available

wires of high purity. Prior to their use, these materials were run for some time at high temperatures under a vacuum until well outgassed.

2.2.2 Deposition System

The pumping system is a Veeco VS-400 module with a Welch 1397B roughing pump. The system employs a liquid nitrogen cold trap. The gaging is done by a Veeco module which consists of one ion gage and two thermocouple gages. The chamber is a special cylindrical unit fabricated around a Varian spool collar. A four inch pumping port is located on one side of the collar so that the entire top and bottom areas are available for unrestricted placement of internal fixturing. The collar itself provides seven ports for electron gun and accessory mounting. Further access is provided through the top and bottom plates. The jar is an open ended cylinder. All chamber seals are either viton or copper. The electron gun is a three-crucible Varian assembly. This unit is capable of delivering 2 KW beam power. The cold substrate deposition apparatus used in conjunction with this equipment is the Librascope design and fabrication.

2.2.3 Monitoring

The resistance of a separate monitor film is measured as the film is deposited. The resistance is determined by passing a constant current through the monitor film and measuring the voltage drop across the film. A current source is created by connecting a large-valued resistor in series with a 90 volt battery. A 12 volt zener diode is connected across the output terminals so the open circuit voltage will be limited. A self contained, high impedance millivoltmeter is connected across the output terminals. The output voltage is proportional to the resistance when the proper multiplying factor is used. During the calibration procedure, a precision resistor of the value to be deposited is connected across the monitor piece terminals and the monitor is set to the desired end point.

As the deposited film thickness on the monitor increases, the meter

reading approaches the predetermined value. Deposition is halted manually when the desired value of resistance is reached. Resistance values from one ohm to 100 kiloohms have been monitored by the means described.

2.2.4 Photoresist Equipment

All photoresist work is done in a room under positive atmospheric pressure and with filtered air inlets. This room is lighted with gold fluorescent tubes to prevent the photoresist from fogging. Critical steps are performed in positive-pressure cabinets which are filtered to provide white conditions. The equipment used includes a Transmask whirling table and a K&S alignment machine. There is a separate closeable booth for spray development. This includes air brushes and a special gas supply system to provide dried and filtered nitrogen. Optical microscopy, including a large screen comparator, is available in the room. Dust-free ovens with good temperature tracking are available for pre-and post-baking.

2.3 TEST EQUIPMENT AND PROCEDURES

This section describes the test equipment and procedures used in making measurements on the resistor samples, and in environmentally stressing them.

2.3.1 Resistance

Resistance values were taken at room temperature on an ESI resistance bridge. The bridge used was a model 250 DA, which reads five places for resistors for which the first two significant figures are either 11 or 10, and reads four places for all other values. There is a possible reading error of about $\pm$ 3 in the last place.

2.3.2 Current Noise

Current noise measurements are made with a system consisting of an audio oscillator, a microvolter, a d-c source, a sample box, a low-noise preamplifier, a narrow-band filter and meter, a rectifier and

filter, and a strip chart recorder.

The audio oscillator and microvolter are used to supply a calibrating signal to the system. They are not connected during the actual run.

The system used for the actual test is the d-c supply, the sample box (with load resistor), the low-noise preamplifier, the filtering and rectifying modules, and the strip chart recorder.

System gain is adjusted to read one microvolt output on the meter for one microvolt input. The center band of the system is 480 cycles with a 38 cycle noise equivalent band width (rectangular band width). The load and sample resistors are connected into the circuit and a system noise reading (no bias voltage) is taken for a minimum of one minute. Bias voltage is applied and a reading for at least one minute is taken. The resulting data are then mathematically processed to give noise per decade in db to the index of

$$\frac{1\ \mu\ \text{volt (RMS)}}{\text{volt (DC)}}$$

This procedure is as follows: First, the mean values of system noise (N_S) and total noise (N_T) are read from the strip chart. Resistor noise (N_R) is found from

$$N_R = \frac{R_X + R_L}{R_L} \sqrt{N_T^2 - N_S^2}$$

where R_X = Resistance of specimen; R_L = load resistance; N_R = open circuit resistor noise voltage.

N_R is then expanded to 1 decade. In this case, the multiplier is 5.5. The result is N_D (noise per decade) in microvolts. This is then converted to db to the index of 1 microvolt per volt.

2.3.3 Temperature Coefficient

A dynamic tester is desirable to facilitate the testing of a large number of samples. A system has been devised which measures and records environmental temperature and percentage change of resistance of the sample simultaneously.

A two channel strip chart recorder is used to record the two parameters in real time. A thermocouple is attached to the resistor substrate, and the output connected to a compensating circuit. Here, a voltage is added to the thermocouple output, corresponding to the difference voltage between 0°C and room temperature. The combined voltages are fed to the recorder. A transistorized constant current generator is connected to the resistor being tested. The current is adjusted to cause an IR drop equal to that of a mercury battery which is connected in series opposition. The resulting output, which is zero at room temperature, is connected to the recorder. The scaling of the recorder is such that a 1% change of resistance will cause a full scale deflection. Other scaling is readily available.

Samples have been measured from room temperature up to both 125°C and 145°C. A few check runs have been made to a negative temperature (-30°C). A test run requires approximately 30 minutes and results in a chart showing the temperature and percentage change in resistance in the same time base. This system does not have the accuracy of bridge measurements, but does serve to establish trend and identify gross temperature-sensitive characteristics with a good degree of precision. It does so at a great saving in test time.

2.3.4 Temperature Stability

The test used for temperature stability is a simple storage test of 100 hours at 145°C. The only equipment required is a laboratory oven. Resistance is measured by a bridge at room temperature before and after the runs.

2.3.5 Moisture Stability

The test used for moisture stability is storage for 48 hours at 100% humidity and room temperature. A constant vapor pressure solution with an equilibrium at 100% humidity is used.

2.4 RAW TEST DATA

The bulk of the data referred to in this section consists primarily of tables of raw or slightly reduced test data. Each table is organized chronologically in the order of sample preparation. Only a fraction of the available samples were subjected to any given test. These samples were selected on a basis of the parameter being studied at the time. A total evaluation of all samples for all parameters would have far exceeded the funded scope of the present contract.

2.4.1 Resistance and Uniformity

The raw resistance data is given in Table I. These data have been reduced to show mean and median values. Numerical and percentage deviations from these values are shown.

2.4.2 Current Noise

The measured data for the calculation of current noise is given in Table II. These data are for a 28 cycle bandwidth. The data are later presented in a converted form which gives noise per decade. (See Table VI).

2.4.3 Temperature Coefficient

These data are presented in Table III. The original data were in terms of millivolts for both temperature and resistance change. These figures have been converted to a temperature span in degrees centigrade, percent change in resistance for that span, temperature coefficient of resistance in parts per million per degree centigrade. All of the data presented in this table are from room temperature upward. A few isolated samples were tested from room temperature down to -30°C in order to prove the operating range. Representative values of TCR for the negative range

are 52 ppm/°C for 100 ohms/square resistance and 105 ppm/°C for 1000 ohms/square resistance.

2.4.4 Temperature Stability

Table IV gives readings taken by a bridge before and after the 100 hour thermal stressing of selected samples. These values have been processed to give the delta R and percent change columns.

2.4.5 Moisture Stability

Bridge measurements, values of delta R and percent change of resistance are given in Table V for the moisture tests.

2.5 EVALUATION OF TEST DATA VERSUS DESIGN GOALS

The purpose of this program was to determine the feasibility of using the cold substrate deposition process to prepare passive devices (resistors and capacitors) for thin film circuitry. In this section, the results obtained are discussed in terms of the design goals. The design goals are listed in Appendix 1.

2.5.1 Sheet Resistance

The sheet resistance specification states that resistors shall be fabricated in the 10^2, 10^3, 10^4 and 10^5 ohms per square ranges. Resistors were prepared for all four ranges and specific design goals for these are discussed in the following paragraphs of Section 2.5.

2.5.2 Temperature Coefficient

The design goal of less than 100 PPM/°C for TCR was met for both 10^2 ohms per square and 10^3 ohms per square, specific examples being substrates 66A16 and 66A17. It was not met for 10^4 ohms per square and 10^5 ohms per square. The best value obtained for 10^4 ohms per square was -476 PPM/°C on substrate 66A45. Values for high resistance devices ranging from -476 to -833 PPM/°C are given in Table III.

2.5.3 Operating Temperature

Samples of all four values of sheet resistance have been evaluated between -30 and +145°C. These samples have been run at these temperatures under light load, and have been returned to room temperature. None of the devices failed, thereby fulfilling the operating temperature design goal for this program.

2.5.4 Adjustment of Resistor Values

The adjustment made on the low resistance sample, as described in Section 2.1.6, could have been made on a sample of any sheet resistance, since it is a matter of geometry only. The four resistors on this substrate (No. 66A12) prior to adjustment were 66.2, 67.3, 67.3 and 64.2 ohms. The target value selected was 70 ohms. The result was $\pm$ 0.12% from a median of 69.9 ohms. The final adjustment could have been carried slightly further to an estimate 70 ohms $\pm$ 0.1%. This fulfills the design goal of +1% regarding adjustment of individual resistors.

2.5.5 Current Noise

Noise requirements were fully met for resistors having sheet resistances of 10^2 and 10^3 ohms per square (for instance substrates 66A14, 66A16, 66A17, and 66A46). The best noise value attained for a sheet resistance in excess of 10^4 ohms per square was -24.5 db on substrate 66A75 (1), which very nearly meets the design goal of 25 db. Noise figures for devices having a sheet resistance of 10^5 ohms per square or more fell short of the design.

2.5.6 Nominal Value

This parameter is more difficult to meet at the higher values of resistance than for 10^2 and 10^3 ohms per square (see data in Table I for substrates 66A16, 66A29, 66A17 and 66A23); it has been met for more than one substrate of each of these two values, all resistors on the substrate being well within tolerance. For 10^4 ohms per square it has

been met for three resistors on a substrate in several instances. Suitable resistance spreads for resistors, slightly in excess of 10^4 ohms per square, have been attained for all four resistors on a substrate. The best example of 10^5 ohms per square is substrate 66A55 which missed meeting the $\pm$ 10% criterion by 0.1% for one resistor. The other three were all within tolerance of 10^5 ohms $\pm$ 10%. The best spread on a resistor substrate in excess of 10^5 ohms per square (actually 1.6×10^5) was $\pm$ 3.6%.

The resistance monitoring system used for this program was set up with a manual link for shutter control. Using manual control, it was possible to reach monitor values well within $\pm$ 10% of the desired value in most instances. For any type of production run, an automatic linkage would be installed.

Using the manual link, it was possible to deposit individual resistors, within the + 10% design goal for all ranges. Using an automatic link, it should be possible to repeat values to $\pm$ 1%, since there is a variable operator reaction time when the manual link is used, and since deposition times are very short. The apparant discrepencies between the target value and the monitor value for many specimens listed in TableI are a consequence of the operator reaction time variable.

2.5.7 Temperature Stability

This design goal specifies a temperatue stability of $\pm$ 2%. The test conditions were 100 hours at 145°C. The goal was met for 10^2 and 10^3 ohms per square resistors (for example, substrates 66A05 and 66A17), but was not met for 10^4 and 10^5 ohms per square resistors.

2.5.8 Moisture Stability

The moisture stability goal of $\pm$ 1% has been met for resistors of all four ranges. Many resistors evaluated displayed negligible change (considerably less than 0.1%). The samples were subjected to 100% relative humidity at room temperature for 48 hours. This is largely a test of the integrity of the protective coating. For exact values, note the data on substrate 0411C, 66A49, 66A41, and 66A52 inTable V.

TABLE I

Resistance Data

(Samples Listed in Chronological Sequence)

Run No.	Sample No.	Monitor and Target Values*** (Ohms)****	Resistance (Ohms)****	Spread** From Median	Spread** From Mean
1	0421 B (Poor edge resolution no SiO backing)	90_2 (10^2)	1)* 116**	(130.5)	(124.8)
			2) 112	±18.5 ohms	+24.2 -12.8 ohms
			3) 122	±13.7%	+19.4% -10.3%
			4) 149		

* These numbers refer to four resistors on a substrate.

** The median and mean values are given in parentheses.

*** Apparent discrepancy between monitor and target values are a consequence primarily of the operator reaction-time variable for the manually operated shutter mechanism.

**** Because of square resistor geometry used, these values are both "resistance" (ohms) and "sheet resistance" (ohms per square).

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
2	0411C	100 ohms (10^2)	1) 116.0	(117.4)	(117.3)
			2) 113.9	± 3.5 ohms	+ 3.6 -3.4 ohms
			3) 119.6	± 2.98%	+ 3.06% -2.9%
			4) 120.9		
3	0411B (Poor edge resolution no SiO backing)	88 ohms (10^2)	1) - - - No measurements recorded. - - -		
			2)		
			3)		
			4)		
4	0411D	100 ohms (10^2)	1) 128.2	(130.15)	(129.05)
			2) 127.7	± 6.65 ohms	+ 7.75 -5.55 ohms
			3) 123.5	± 5.1%	+ 6% -4.3%
			4) 136.8		
5	66A03 (Tab Material Only Ti-Cu-Ni)	None	1) 15.8	(17.05)	(17.25)
			2) 17.5	± 1.35 ohms	+ 1.05 -1.45 ohms
			3) 18.3	± 7.9%	+ 6.1% -8.4%
			4) 17.3	This establishes a possible measurement error of about 2 ohms in making probe contacts to samples. To be noted with regard to 100 ohm samples.	

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
6	66A06 (Sector shutter added)	100 ohms (10^2)	1) 114 2) 108 3) 105 4) 110	(109.5) $\pm$ 4.5 ohms $\pm$ 4.1%	(109.2) +4.8 -4.2 ohms +4% -3.9%
7	66A07	100 ohms (10^2)	1) 148.8 2) 133.4 3) 129.4 4) 144.2	(139.1) $\pm$ 9.7 ohms $\pm$ 7%	(139.0) +9.8 -9.6 ohms +7.1% -6.9%
7	66A02	(10^2)	1) 113.9 2) 123.6 3) 119.8 4) 119.6	(118.85) $\pm$ 4.85 ohms $\pm$ 4.1%	(119.22) +5.3 -4.4 ohms +4.4% -3.7%
8	66A04	100 ohms (10^2)	1) 86.0 2) 100.0 3) 105.3 4) 87.7	(95.65) $\pm$ 9.65 ohms $\pm$ 10.1%	(96.8) +8.5 -10.8 ohms +8.8% -11.2%

Table I(cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
8	66A10	(10^2)	1) 91.9	(108.95)	(100.95)
			2) 127.3	± 13.4 ohms	+ 26.4 -10.4 ohms
			3) 90.6	± 12.3%	+ 26.2% -10.3%
			4) 94.0		
9	66A05	100 ohms (10^2)	1) 114	(113.5)	(113.25)
			2) 109	± 4.5 ohms	+ 4.8 -4.2 ohms
			3) 114	± 4%	+ 4.2% -3.6%
			4) 118		
9	66A08	(10^2)	1) 154	(146.5)	(145.8)
			2) 144	± 7.5 ohms	+ 18.2 -6.8 ohms
			3) 139	± 5.1%	+ 5.6% -4.7%
			4) 146		
10	66A01	100 ohms (10^2)	1) 111.4	(110.0)	(111.0)
			2) 106.7	± 3.35 ohms	+ 2.4 -4.3 ohms
			3) 112.5	± 3%	+ 2.2% -3.9%
			4) 113.4		

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
11	66A16	No record. (10^2)	1) 96.3 2) 104.4 3) 94.4 4) 91.2	(96.8) $\pm$ 6.6 ohms $\pm$ 6.8%	(96.1) +8.3 -4.9 ohms +8.6% -5.1%
12	66A20	No record (10^2)	1) 79.1 2) 84.7 3) 79.5 4) 74.6	(79.6) $\pm$ 5 ohms $\pm$ 6.3%	(79.5) +5.2 -4.9 ohms +6.5% -6.2%
13	66A14	100 ohms (10^2)	1) 90.5 2) 95.8 3) 96.5 4) 86.1	(91.3) $\pm$ 5.2 ohms $\pm$ 5.7%	(92.2) +4.3 -6.1 ohms +4.7% -6.6%
14	66A12	100 ohms (10^2)	1) 66.2 2) 67.3 3) 67.3 4) 64.2	(65.8) $\pm$ 1.6 ohms $\pm$ 2.5%	(66.2) +1.1 -2 ohms +1.7% -3%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
15	66A15	100 ohms (10^2)	1) 139.2 2) 151.4 3) 146.1 4) 132.7	(142.0) $\pm$ 9.4 ohms $\pm$ 6.6%	(142.6) +8.8 -9.9 ohms +6.2% -7%
16	66A19	100 ohms (10^2)	1) 132.7 2) 141.5 3) 137.0 4) 128.1	(134.8) $\pm$ 6.7 ohms $\pm$ 5%	(134.8) $\pm$ 6.7 ohms $\pm$ 5%
17	66A11 (New substrate holder)	100 ohms (10^2)	1) 141.1 2) 147.9 3) 143.4 4) 137.2	(142.6) $\pm$ 5.4 ohms $\pm$ 3.8%	(142.8) +5.2 -5.6 ohms +3.7% -3.9%
18	66A18 (Leak located and repaired after)	Not recorded. (10^2)	1) >100,000* 2) 119.8 3) 119.4 4) 145.1	(132.2) (3) $\pm$12.8 ohms $\pm$ 9.7%	(128.1) (3) +17 -8.7 ohms +13.3% -6.8%

* This value not used in calculating spread data.

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
19	66A17	800 ohms (10^3)	1) 969.2 2) 922.0 3) 960.0 4) 1,034	(978.0) ± 56 ohms ± 5.7%	(971.3) + 62.7 -49.3 ohms + 6.5% -5.1%
20	66A23	900 ohms (10^3)	1) 973.9 2) 990.9 3) 1,063 4) 960	(1011.5) ± 51.5 ohms ± 5.1%	(999.4) + 63.6 -39.4 ohms + 6.4% -3.9%
21	66A29 (Screen added)	100 ohms 10^2)	1) 109.0 2) 109.0 3) 108.7 4) 108.3	(108.6) ± 0.4 ohms ± 0.37%	(108.8) + 0.2 -0.5 ohms + 0.18% -0.46%
22	66A13	1000 ohms (10^3)	1) 811 2) 860 3) 1,640 4) open°	(1225.5) (3) ± 414.5 ohms ± 33.8%	(1103.7) (3) + 536.3 -292.6 ohms + 49% -26.5%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
23	66A37	1000 ohms (10^3)	1) 1,120	(1195.2)	(1069.4)
			2) 1,672	± 476.8 ohms	+602.6 -351.0 ohms
			3) 718.4	± 40%	+56% -33%
			4) 767.0		
24	66A31	1000 ohms (10^3)	1) 1,244	(1152) (2)	(1152) (2)
			2) 200,000 °	± 92 ohms	± 92 ohms
			3) open °	± 8%	± 8%
			4) 1,060		
25	66A48	Open (10^2)	1) 147.2	(146.8)	(147.0)
			2) 147.2	± 1.25 ohms	+1 -1.5 ohms
			3) 145.5	± 0.85%	+0.68% -1.02%
			4) 148.0		
26	66A46	Open (10^3)	1) 892.5	(845.9)	(850.1)
			2) 937.8	± 91.9 ohms	+87.7 -96.1 ohms
			3) 816.1	± 10.9%	+10.3% -11.3%
			4) 754.0		

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
27	66A49	1001 ohms (10^3)	1) 1,049	(1091.8)	(1092.7)
			2) 1,253	±160.2 ohms	+160.3 -162 ohms
			3) 1,138	±14.7%	+14.7% -14.8%
			4) 930.7		
28	66A47	10,100 ohms (10^4)	1) 19,000	(30,590)	(28,025)
			2) 42,180	±11,590 ohms	+14,155 -9,025 ohms
			3) 26,000	±32%	+50.5% -32%
			4) 24,930		
28	66A42	(10^4)	1) 6,950	(8,066)	(7,578)
			2) 7,232	±2,244 ohms.	+2,732 -1,757 ohms
			3) 10,310	±26%	+36% -23%
			4) 5,821		
29	66A44	9,945 ohms (10^4)	1) 7,617	(7649.5) (2)	(7649.5) (2)
			2) 700,000°	±32.5 ohms	±32.5 ohms
			3) 260,000°	±4.25%	±4.25%
			4) 7,682		

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
30	66A41	10, 235 ohms (10^4)	1) 7, 832 2) 17, 450 3) 9, 874 4) 8, 865	(12, 641) $\pm$4, 809 ohms $\pm$38%	(11, 005) +6, 445 -3, 173 ohms +58.5% -28.9%
31	66A45	10, 700 ohms (10^4)	1) 10, 326 2) 22, 120 3) 10, 275 4) 9, 875	(15, 998) $\pm$6122 ohms $\pm$38%	(13, 149) +8981 -3266 ohms +68.5% -25%
32	66A51	10, 600 ohms (10^4)	1) 14, 740 2) 13, 810 3) 16, 890 4) 43, 520	(38, 665) $\pm$14, 855 ohms $\pm$52%	(22, 240) +21, 280 -8, 430 ohms +96.5% -38%
33	66A52	94, 450 ohms (10^5)	1) 93, 315 2) 67, 260 3) 84, 605 4) 617, 700°	(80, 288) (3) $\pm$13, 028 ohms $\pm$16.3%	(81, 727) (3) +11, 588 -14, 467 ohms +14.1% -17.6%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
34	66A53	147, 200 ohms (10^5)	1) 117, 600 2) 136, 900 3) 138, 500 4) 120, 300	(128, 050) $\pm$ 10, 450 ohms $\pm$ 8. 2%	(128, 325) + 10, 175 -10, 725 ohms + 7. 9% -8. 4%
35	66A54	105, 000 ohms (10^5)	1) 154, 700 2) 162, 500 3) 166, 400 4) 166, 300	(160, 550) $\pm$ 5, 850 ohms $\pm$ 3. 6%	(162, 475) + 3, 925 -7, 775 ohms + 2. 4% -4. 8%
36	66A55	98, 000 ohms (10^5)	1) 99, 700 2) 110, 100 3) 101, 700 4) 92, 500	(101, 300) $\pm$ 8, 800 ohms $\pm$ 8, 7%	(101, 000) + 9100 -8500 ohms + 9% -8. 4%
37	66A56	8, 985 ohms (10^4)	1) 7, 473 2) 8, 026 3) 11, 415 4) 7, 324	(9, 370) $\pm$ 2, 046 ohms $\pm$ 21. 8%	(8, 560) + 2, 855 -1, 236 ohms + 33. 4% -14. 4%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
38	66A57	9,673 ohms (10^4)	1) 10,300 2) 11,755 3) 10,200 4) 9,280	(10,517) $\pm$ 1,238 ohms $\pm$ 11.7%	(10,384) +1,371 -1,104 ohms +13.2% -10.6%
39	66A58	1,027 ohms (10^3)	1) 1,060 2) 1,137 3) 1,078 4) 1,032	(1,084) $\pm$ 53 ohms $\pm$ 4.9%	(1,077) +60 -45 ohms +5.6% -4.2%
40	66A59	10,060 ohms (10^4)	1) 7,055 2) 7,855 3) 7,100 4) 7,208	(7,455) $\pm$ 400 ohms $\pm$ 5.4%	(7,304) +551 -249 ohms +7.6% -3.4%
41	66A60	10,090 ohms (10^4)	1) 15,850 2) 20,000 3) 20,000 4) 18,640	(17,925) $\pm$ 2,075 ohms $\pm$ 11.6%	(18,622) +1,378 -2,772 ohms +7.4% -14.6%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
42	66A61	8, 329 ohms (10^4)	1) 5, 773 2) 78, 940 3) 10, 000, 000 4) open	not meaningful	not meaningful
43	66A62	27, 350 ohms (10^4)	1) 3, 610 2) open° 3) open° 4) 5, 639	(4, 624) (2) ± 1, 015 ohms ± 22%	(4, 624) (2) ± 1, 015 ohms ± 22%
44	66A63	10, 568 ohms (10^4)	1) 7, 292 2) 7, 706 3) 7, 403 4) 6, 912	(7, 309) ± 397 ohms ± 5.4%	(7, 328) + 378 -416 ohms + 5.2% -5.7%
45	66A64	8, 415 ohms (10^4)	1) 6, 326 2) 6, 788 3) 6, 625 4) 6, 250	(6, 519) ± 269 ohms ± 4.1%	(6, 398) + 390 -148 ohms + 6.1% -2.3%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
46	66A65	Open (10^4)	1) 13, 410 2) 14, 430 3) 12, 710 4) 13, 790	(13, 570) $\pm$860 ohms $\pm$6.3%	(13, 585) +845 -875 ohms +6.2% -6.4%
47	66A66	Open (10^3)	1) 742.8 2) 762.0 3) 900, 000° 4) 750.0	(752.4) (3) $\pm$9.6 ohms $\pm$1.3%	(751.6) (3) +10.4 -8.8 ohms +1.4% -1.2%
48	66A67	10, 639 ohms (10^4)	1) 10, 532 2) 11, 680 3) 11, 003 4) 9, 526	(10, 603) $\pm$1, 077 ohms $\pm$10.1%	(10, 685) +995 -1, 159 ohms +9.3% -10.9%
49	66A68	Not recorded (10^4)	1) 13, 400 2) 12, 800 3) 11, 100 4) 9, 000	(11, 200) $\pm$2, 200 ohms $\pm$19.7%	(11, 574) +1, 826 -2, 574 ohms +15.8% -22.2%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
50	66A69	9,098 ohms (10^4)	1) 6,639 2) 6,879 3) 6,181 4) 6,318	(6,530) ± 349 ohms ± 5.4%	(6,504) +375 -323 ohms +5.8% -5%
51	66A70	13,300 ohms (10^4)	1) 7,554 2) 6,818 3) 6,895 4) 6,840	(7,186) ± 368 ohms ± 5.1%	(7,027) +527 -209 ohms +7.5% -3%
52	66A71	Not recorded (10^3)	1) 4,260 2) 3,970 3) 3,750 4) 3,900	(4,005) ± 255 ohms ± 6.4%	(3,970) +290 -220 ohms +7.7% -5.8%
53	66A72	Not recorded (10^4)	1) 8,475 2) 7,420 3) 8,160 4) 10,510	(8,965) ± 1,545 ohms ± 17.3%	(8,641) +1,869 -1,221 ohms +21.7% -14.2%

Table I (cont'd)

Run No.	Sample No.	Monitor and Target Values (Ohms)	Resistance (Ohms)	Spread From Median	Spread From Mean
54	66A73	Not recorded (10^4)	1) 5, 330 2) 4, 400 3) 4, 540 4) 5, 710	(5, 055) ± 655 ohms ± 13%	(4, 995) + 715 -595 ohms + 14. 3% -12%
55	66A74	5, 620 ohms (10^4)	1) 19, 700 2) 22, 300 3) 29, 300 4) 25, 300	(24, 500) ± 4, 800 ohms ± 19. 6%	(24, 150) + 5, 150 -4, 450 ohms + 21. 4% -18. 5%
56	66A75 (1)	9, 240 ohms (10^4)	1) 25, 500 2) 15, 000 3) 14, 200 4) 30, 000	(22, 100) ± 7, 900 ohms ± 35. 8%	(21, 175) + 8, 825 -6, 975 ohms + 40. 5% -32%
56	66A75 (2)	(10^4)	1) 9, 820 2) 9, 830 3) 17, 300° 4) 9, 700	(9, 765) (3) ± 65 ohms ± 0. 67%	(9, 783) (3) + 47 -83 ohms + 0. 48% -0. 85%

TABLE II

Noise Data

Sample Number		System Noise (μV)	Total Noise (μV)	DC Voltage (Volts)	R Load (Ohms)
0411C	1*	0.06	0.07	3.6	1,100
(10^2)**	2	0.06	0.068	3.5	1,100
	3	0.06	0.072	3.6	1,100
	4	0.06	0.083	3.6	1,100
0411D	1	0.06	0.062	6.0	1,100
(10^2)	2	0.06	0.066	6.0	1,100
	3	0.06	0.068	6.0	1,100
	4	0.06	0.07	6.0	1,100
66A06	1	0.058	0.068	3.5	1,100
(10^2)	2	0.059	0.064	3.2	1,100
	3	0.059	0.07	3.2	1,100
	4	0.058	0.068	3.4	1,100
66A04	1	0.058	0.070	4.0	1,100
(10^2)	2	0.058	0.087	4.4	1,100
	3	0.058	0.100	4.5	1,100
	4	0.058	0.100	4.0	1,100
66A05	1	0.058	0.066	4.5	1,100
(10^2)	2	0.058	0.085	3.2	1,100
	3	0.060	0.087	3.4	1,100
	4	0.060	0.063	5.3	1,100
66A01	1	0.06	0.08	1.7	1,100
(10^2)	2	0.06	0.068	2.6	1,100
	3	0.058	0.062	5.4	1,100
	4	0.058	0.065	5.2	1,100
66A16	1	0.115	0.115	3.8	1,100
(10^2)	2	0.115	0.115	4.0	1,100
	3	0.115	0.120	3.8	1,100
	4	0.110	0.110	3.7	1,100

* Four resistors per substrate.

** Sheet resistance range.

Table II cont.

Sample Number		System Noise (μV)	Total Noise (μV)	DC Voltage (Volts)	R Load (Ohms)
66A20	1	0.110	0.110	3.6	1,100
(10^2)	2	0.110	0.110	3.8	1,100
	3	0.110	0.110	3.6	1,100
	4	0.110	0.110	3.4	1,100
66A14	1	0.085	0.085	3.8	1,100
(10^2)	2	0.08	0.08	3.8	1,100
	3	0.08	0.08	3.7	1,100
	4	0.08	0.08	3.3	1,100
66A17	1	0.065	0.065	10	10,000
(10^3)	2	0.067	0.067	10	10,000
	3	0.067	0.070	10	10,000
	4	0.067	0.072	10	10,000
66A23	1	0.13	4.5	6	1,100
(10^3)	2	0.125	6.0	5	1,100
	3	0.125	55	5	1,100
	4	0.125	35	5	1,100
66A29	1	0.11	0.15	3.5	1,100
(10^2)	2	0.11	0.135	3.5	1,100
	3	0.11	0.12	3.5	1,100
	4	0.11	0.112	3.5	1,100
66A48	1	0.06	0.08	4.6	1,100
(10^2)	2	0.06	0.075	4.5	1,100
	3	0.06	0.072	4.5	1,100
	4	0.06	0.07	4.5	1,100
66A46	1	0.12	0.12	9	1,100
(10^3)	2	0.11	0.14	9	1,100
	3	0.115	0.115	9	1,100
	4	0.115	0.12	9	1,100

Table II cont.

Sample Number		System Noise (μV)	Total Noise (μV)	DC Voltage (Volts)	R Load (Ohms)
66A41	1	0.1	0.55	3.0	10,000
(10^4)	2	0.1	1.2	4.0	10,000
	3	0.1	0.6	3.0	10,000
	4	0.1	0.5	3.0	10,000
66A45	1	0.1	3.7	4.0	10,000
(10^4)	2	0.1	6	4.0	10,000
	3	0.1	2.3	3.0	10,000
	4	0.1	2.2	3.0	10,000
66A54	1	0.1	3.6	0.75	100,000
(10^5)	2	0.1	5.0	0.75	100,000
	3	0.1	7.5	0.75	100,000
	4	0.1	2.3	0.75	100,000
66A63	1	0.1	0.63	4	10,000
(10^4)	2	0.1	0.48	4	10,000
	3	0.1	0.68	4	10,000
	4	0.1	0.64	4	10,000
66A64	1	0.07	0.26	1.0	10,000
(10^4)	2	0.07	0.62	1.0	10,000
	3	0.07	0.95	1.0	10,000
	4	0.07	0.28	1.0	10,000
66A71	1	0.065	0.11	10	10,000
(10^3)	2	0.065	0.115	10	10,000
	3	0.065	0.10	10	10,000
	4	0.065	0.10	10	10,000
66A72	1	0.065	0.27	10	10,000
(10^4)	2	0.065	>1	10	10,000
	3	0.065	0.18	10	10,000
	4	0.065	0.185	10	10,000

Table II cont.

Sample Number		System Noise (μV)	Total Noise (μV)	DC Voltage (Volts)	R Load (Ohms)
66A73	1	0.065	>1	10	10,000
(10^4)	2	0.065	0.84	10	10,000
	3	0.065	0.55	10	10,000
	4	0.065	0.85	10	10,000
66A75 (1)	1	0.22	0.37	30	10,000
(10^4)	2	0.23	0.30	40	10,000
	3	0.23	0.32	50	10,000
	4	0.22	0.29	40	10,000

TABLE III

Temperature Coefficient of Resistance

Sample Number		Temperature Span (°C)**	% Change in Resistance	PPM/°C
0411D	1	71	0.48	69
(10^2)*	3	80	0.48	60
66A06	1	76	0.36	47
	2	79	0.64	81
66A04	3	78	0.40	51
(10^2)				
66A05	1	77	0.72	94
(10^2)	3	80	0.66	83
66A01	1	67	1.0	150
(10^2)	4	82	0.56	68
66A16	1	122	1.04	87
(10^2)	2	120	1.24	103
	3	122	0.70	58
	4	119	0.54	45
66A20	1	122	1.1	90
(10^2)	2	120	1.14	95
	3	78	0.54	70
	4	128	0.70	55
66A14	1	78	1.04	133
(10^2)	2	115	1.12	97
	3	73	1.2	167
	4	117	1.12	96
66A17	1	78	0.88	113
(10^3)	2	124	1.0	81
	3	127	1.08	85
	4	124	1.00	81

* Sheet resistance range.

** The temperature span (initial value is room temperature and final value is an elevated temperature) over which the % change in resistance was measured.

Table III cont.

Sample Number		Temperature Span (°C)	% Change in Resistance	PPM/°C
66A23	1	51	0.58	114
(10^3)	2	72	0.96	134
	3	73	0.98	134
66A29	1	121	0.74	60
(10^2)	2	122	0.54	44
	3	117	0.46	39
	4	125	0.58	46
66A41	1	21	1.0	476
(10^4)	3	15	0.95	635
66A45	1	13	1.0	770
(10^4)	2	12	1.0	833

TABLE IV

Temperature Stability
(100 hours at 145°C)

Sample Number		Before	After	Δ R	% Change
0411C	1 *	116.0 ohms	114.2 ohms	-1.8 ohms	-1.5
(10^2)**	2	113.9	111.8	-2.1	-1.9
	3	119.6	116.5	-3.1	-2.6
	4	120.9	118.5	-2.4	-2.0
0411D	1	128.2	127.2	-1.0	-0.8
(10^2)	2	127.7	126.2	-1.5	-1.2
	3	123.5	122.5	-1.0	-0.8
	4	136.8	123.8	-3.0	-2.2
66A06	1	114.1	114.5	+0.4	+0.4
(10^2)	2	107.6	109.0	+1.4	+1.3
	3	104.8	106.0	+1.2	+1.1
	4	109.8	110.0	+0.2	+0.2
66A04	1	86.0	83.8	-2.8	-3.3
(10^2)	2	100.1	95.0	-5.1	-5.1
	3	105.3	98.2	-7.1	-6.7
	4	87.7	85.4	-2.3	-2.6
66A05	1	112.4	112.5	-0.1	-0.1
(10^2)	2	107.1	107.5	+0.4	+0.4
	3	111.9	111.5	-0.4	-0.4
	4	117.5	117.4	-0.1	-0.1
66A01	1	111.4	109.0	-2.4	-2.2
(10^2)	2	106.7	104.5	-2.2	-2.1
	3	112.5	110.0	-2.5	-2.2
	4	113.4	110.5	-2.9	-2.6
66A14	1	90.0	90.0	0	0
(10^2)	2	95.2	94.8	-0.4	-0.4
	3	95.6	95.4	-0.2	-0.2
	4	85.5	85.2	-0.3	-0.4

* Four resistors per substrate.
** Range.

Table IV cont.

Sample Number		Before	After	ΔR	% Change
66A17	1	987	1007	+20	2.0
(10^3)	2	940	958	+18	1.8
	3	990	1000	+10	1.0
	4	1054	1070	+16	1.6
66A23	1	1021	1182	+161	16.1
(10^3)	2	1001	1320	+319	31.9
	3	1080	1420	+340	34
	4	1020	1650	+630	63
66A46	1	890	858	-32	3.6
(10^3)	2	932	890	-42	4.5
	3	810	778	-32	3.9
	4	751	724	-28	3.7

TABLE V

Moisture Stability
(48 hours, 100% relative humidity, room temperature)

Sample Number		Before	After	Δ R	% Change
0411C	1*	113.8 ohms	114.3 ohms	+0.5 ohms	+0.4
(10^2)**	2	112.2	112.0	-0.2	-0.2
	3	116.7	116.8	+0.1	-0.1
	4	118.4	118.4	- 0 -	- 0 -
66A23	1	982.8	984.7	+1.9	+0.2
(10^3)	2	992.6	998.0	+5.4	+0.5
	3	1066.7	1087.0	+20.3	+1.9
	4	968.5	980.5	+12.0	+1.2
66A37	1	980	980	- 0 -	- 0 -
(10^3)	2	1700	1100	-600	-35.0
	3	720	720	- 0 -	- 0 -
	4	768	773	+5.0	+0.65
66A48	1	146.1	146.2	+0.1	+0.1
(10^2)	2	146.1	146.3	+0.2	+0.2
	3	144.8	145.1	+0.3	+0.2
	4	147.6	147.7	+0.1	+0.1
66A49	1	1044	1044	- 0 -	- 0 -
(10^3)	2	1245	1245	- 0 -	- 0 -
	3	1010	1010	- 0 -	- 0 -
	4	927	928	- 0 -	- 0 -
66A41	1	7,686	7,790	+104	+1.4
(10^4)	2	16,820	17,005	+185	+1.1
	3	9,637	9,715	+78	+0.8
	4	8,863	9,149	+286	+3.2
66A52	1	105,210	109,200	+3,990	+3.8
(10^5)	2	74,260	75,800	+1,540	+2.1
	3	93,300	93,100	-200	-0.2
	4	660,000	656,000	-4,000	-0.6

* Four resistors per substrate.
** Range.

TABLE VI

Current Noise - Calculated Values (per decade)

Sample Number		Noise, db, Index 1 μ volt per volt	Sample Number		Noise, db, Index 1 μ volt per volt
0411C	1 *	-25	66A20	1	-37.3
(10^2)**	2	-25	(10^2)	2	-36.8
	3	-24		3	-37.3
	4	-30		4	-35.8
0411D	1	-36	6 6A14	1	-36.8
(10^2)	2	-31	(10^2)	2	-36.8
	3	-30		3	-36.6
	4	-30		4	-35.9
66A06	1	-24	66A17	1	< -45
(10^2)	2	-27	(10^3)	2	< -45
	3	-23		3	-39
	4	-24		4	-34
66A04	1	-25	66A23	1	+6
(10^2)	2	-21	(10^3)	2	-0.44
	3	-19		3	+1.8
	4	-18		4	+8.8
66A05	1	-28	66A29	1	-16
(10^2)	2	-19	(10^2)	2	-18
	3	-19		3	-21
	4	-34		4	-25
66A01	1	-14.5	66A48	1	-23
(10^2)	2	-22.7	(10^2)	2	-25
	3	-32		3	-25
	4	-29		4	-27
66A16	1	-35	66A46	1	-44.7
(10^2)	2	-32	(10^3)	2	-29.4
	3	-34.5		3	-28.6
	4	-28.7		4	-40.4

* Four resistors per substrate.

** Range.

Table VI cont.

Sample Number		Noise, db, Index 1 μ volt per volt	Sample Number		Noise, db, Index 1 μ volt per volt
66A41	1	+48	66A71	1	-23
(10^4)	2	+10	(10^3)	2	-22.8
	3	+6.8		3	-24.9
	4	+5.1		4	-24.8
66A45	1	+19	66A72	1	-11.6
(10^4)	2	+29	(10^4)	2	-0.36
	3	+18		3	-15.5
	4	+18		4	-14-2
66A54	1	+36.4	66A73	1	-1.4
(10^5)	2	+39.6	(10^4)	2	-4.5
	3	+41		3	-7.8
	4	+33.2		4	-2.9
66A63	1	+3	66A75(1)	1	-14.3
(10^4)	2	+1.1	(10^4)	2	-23.6
	3	+4.2		3	-24.5
	4	+3.5		4	-19.6
66A64	1	+6.8			
(10^4)	2	+15.3			
	3	+18.9			
	4	+7.5			

3.0 CAPACITORS

This section describes the steps taken in the fabrication, by cold substrate deposition, of multiple capacitors of silicon monoxide on a single substrate. The materials involved and the type equipment employed for fabrication, control and test are considered in detail. All significant raw data are tabulated. Finally, an evaluation is presented of the results achieved, as verified by the test data, versus the design goals as summarized in Appendix I.

3.1 FABRICATION PROCEDURES

Two methods of capacitor fabrication were used for this program. Both methods are forms of the cold substrate deposition process. In one case, thermal evaporation was by electron beam heating; in the other case thermal evaporation was by means of resistance heating. Procedures for both methods are outlined. A typical capacitor substrate is shown in Figure 2 on page 5 .

3.1.1 Fabrication With Electron Beam Heating

The basic techniques used for this form of fabrication are those previously described for preparing resistors. There are some minor modifications and, of course, the sequence of operations is different.

3.1.1.1 Base Electrode Deposition

The base electrode used for capacitors was titanium-nickel. The titanium was a thin flash (12-15 seconds); the nickel was relatively thin (10 minutes maximum). Substrate preparation must be very thorough for capacitors, as any roughtness or adhering material can cause a defect in the dielectric layer. All substrates were therefore examined closely before and after the deposition and etching steps.

The procedure used was:

1. Clean and prepare substrates
2. Mount substrates and pump-down system
3. Evaporate SiO layer

4. Vent and clean system
5. Evaporate titanium
6. Evaporate nickel
7. Vent and remove substrates

3.1.1.2 Base Electrode Definition

The procedure used for base electrode definition was the same as that used for conductor definition of resistors. The exact steps of this form of definition are the same as the titanium-nickel case given in Section 2.1.2. The removal of the titanium in the etched areas is even more critical for this application than for resistors.

3.1.1.3 Dielectric Definition

The only definition required in the dielectric layer is to facilitate electrical connection to the base electrodes. This is not necessarily a high resolution masking. Both rejection and mechanical masking were used for this step. The rejection masking procedure used is the one previously described in Section 2.1.3. Mechanical masking is performed using glass masks to shadow an area on the bottom electrodes for later electrical contact. These masks are aligned while mounting the substrates in the substrate holder.

3.1.1.4 Dielectric and Counter Electrode Deposition

The dielectric layer is SiO, deposited through a rotating sector mask. The thickness of deposit is monitored with a crystal-frequency monitor.

It has been found that layered evaporation of the SiO provides a better dielectric. The procedure is to pump down, heat the SiO until evaporation starts, open the shutter, and then vary the e-beam current in a cyclic manner to start and stop SiO evaporation. When the monitor cut-off point is reached, the shutter is closed.

The counter electrode is nickel only, and is deposited directly on the SiO without delay or exposure to atmosphere. The SiO is cooled, the

gun changed to the nickel crucible, and the nickel is briefly outgassed. The shutter is then opened and the nickel layer is deposited.

3.1.1.5 Counter Electrode Definition

The counter electrodes are defined by a photoetch procedure similar to that used for base electrode definition. In this case, the only etchant used is ferric chloride. The hydrofluoric acid etch is not necessary and is eliminated to avoid degradation of the dielectric layer.

3.1.1.6 Trimming

Trimming to reduce capacitance is by selected area etching of the top electrode. This is rather straight forward, and is the same etch as for the original counter electrode definition.

3.1.2 Fabrication with Resistance Heating

A series of capacitors was prepared by the use of resistance heating. This was done in another vacuum station. The substrate used was Corning 9059 glass. The electrode material was aluminum, and the dielectric was SiO.

The electrodes for this series of capacitors were defined by means of metal contact masks. The base electrodes were aluminum applied by cold substrate deposition.

The dielectric layer for these capacitors was SiO deposited from a molecular furnace. Cyclic evaporation, as described in Section 3.1.1, was used to deposit the SiO to obtain a better dielectric layer.

The counter electrodes for these capacitors was aluminum. This deposition was also performed using mechanical masks.

3.2 EQUIPMENT AND MATERIALS FOR FABRICATION

Two different equipment configurations were employed for capacitor fabrication. One was the electron beam station described in Section

2.2.2. For capacitor fabrication this was used in conjunction with a crystal frequency monitor which was fabricated at Librascope.

The other station was an 18-inch bell jar station with a 6-inch NRC pump and liquid nitrogen baffle. This station was equipped with an Edwards optical monitor and with Librascope Cold Substrate Deposition apparatus. Tungsten filaments were used for aluminum evaporation and a baffled boat source for silicon monoxide evaporation.

The materials utilized for capacitor fabrication by electron beam evaporation were all from the group described under materials for resistor fabrication (Section 2.2.1); viz., titanium, nickel, silicon monoxide, and American Lava substrates.

In the resistance heating station, evaporation grade aluminum was used for capacitor electrodes, and in this case, Corning 7059 glass as the substrate material.

3.3 TEST EQUIPMENT AND PROCEDURES

This section outlines the test equipment and procedures employed to determine the characteristics and performance of the thin film capacitors.

3.3.1 Capacitance and Dissipation Factor

Values of capacitance and dissipation factor were checked using the ESI bridge (model 240 DA). The bridge oscillator was consistently set at a peak output of 3 volts for these tests.

3.3.2 Temperature Coefficient

Temperature coefficient tests were conducted with the ESI bridge and a laboratory oven. The tests were not of a dynamic type because of the necessity of manual adjustment of the bridge. Therefore, this operation consisted of taking measurements after temperature stabilization at a series of temperature points.

3.3.3 Stability

To evaluate stability, the specimens were subjected to 145°C for 100 hours. The equipment was a laboratory oven, and the ESI bridge for before-and-after measurements of capacitance and dissipation factor. The devices were also checked for breakdown voltage as described in Section 3.3.5.

3.3.4 Working Voltage

In this program, working voltage is defined as one-half the breakdown voltage. This definition is discussed in the following section. The test equipment and procedures are likewise discussed there.

3.3.5 Breakdown Voltage

During the course of this program, the various methods of establishing voltage specifications for capacitors and dielectric films were scrutinized. In so doing, two definitions of working voltage are apparent. One is based on device survival. In this case, the working voltage is defined as the voltage stress level under which the device will remain stable for a long period of time. Because of the time duration limitations of this program, is was elected not to use this definition as the criterion, but to select the following definition; namely, that the working voltage is one-half the breakdown voltage.

Three methods were employed in investigating the breakdown voltage;

(1) The sample was subjected to a full-wave rectified voltage from a Tektronix 575 CRO. The scope image was monitored for breakdown spikes as the voltage was increased.

(2) This test involved the application of a 100 volt pulse. This was applied through an R-C network with a discharge circuit time-constant of 70 milliseconds. The steady state voltage of the circuit was 50 volts. The applied voltage was therefore a 100 volt pulse, which dropped to a steady 50 volts and remained on the device under test.

(3) This method applied a non-ohmic conduction criterion. The capacitor was subjected to a slowly rising voltage from a saw-tooth function generator. The d-c current through the specimen was measured and the current plotted against voltage on an X-Y plotter. The voltage at which non-ohmic conduction began was read from the plot.

Measurements of all three types were performed on selected samples and comments are accordingly presented (in a later section) in evaluating the capacitors in terms of the design goals. The third method, however, was considered to be the most severe test.

The breakdown voltage in this third context would be defined as "that voltage at which non-ohmic d-c conduction processes begin to occur." In that the onset of non-ohmic d-c conduction occurs somewhat below the point where irreversible changes in the dielectric take place (catastrophic failure), this value is interpreted as a stringent characterization of breakdown voltage. Referring to Table IX, one observes that in some instances a voltage range, rather than a single voltage, is given. This is a consequence of the lack of an abrupt change in the slope of the curve (the "knee") in these cases.

The equipment for the third test method consisted of a Tektronix 5 7 5 scope (sawtooth output), an electronic microammeter, and a Librascope X-Y plotter.

3.4 RAW TEST DATA

This section consists of short discussions and comments on raw test data obtained from capacitor samples.

3.4.1 Capacitance and Dissipation Factor

Table VII lists capacitance and dissipation factor data for all capacitors prepared during this program. Those devices which were shorted during fabrication are so labeled.

3.4.2 Temperature Coefficient of Capacitance

An anomaly of capacitance variation with temperature was found during

the first heating and cooling cycle of these devices. The capacitance values gave an open loop on a plot of capacitance versus temperature. Beginning and ending values at 25°C were the same within limits of measurement error. The rising and descending branches of the curves closed in the range of 75°C to 100°C but, at 50°C, the rising temperature branch showed a capacitance typically 5 to 6% less than capacitance on the decreasing temperature branch. This open loop effect appears to be related to some permanent form of dielectric stabilization (aging), since it appeared only on the first high temperature TCC run. On a second TCC run all devices tested showed a single branch curve with the decreasing temperature branch falling within experimental error of the rising temperature branch. Table VIIIshows the TCC value for two devices on substrate 66C04. All devices on this substrate displayed this general TCC behavior.

3.4.3 Stability

Substrate 66C04 was subjected to 100 hours at 145°C. Capacitance values, measured after the test, showed a reduction of capacitance which averaged 5%. Dissipation factor dropped to about 1/2 the initial value. There was no measureable change in breakdown voltage.

3.4.4 Working Voltage

On the basis of the commencement of non-ohmic conduction, the capacitors on substrate 66C04 are rated at a working voltage between 15 and 30 volts. These same capacitors have all withstood a 100 volt pulse test, and have endured a continuous 50 volt d-c stressing for about 15 minutes. The evidence indicates that there are no destructuve breakdown phenomona below 50 volts.

3.4.5 Breakdown Voltage

The devices on 66C04 and on several of the 66B series substrates were subjected to the 100 volt pulse test without degradation. These devices were also run on the X-Y plotter to determine the onset of non-ohmic conduction. Table IX shows results of tests on five of the devices on

substrate 66C04. Several of the 66B devices were also checked on the Tektronix 575 CRO, and survived 100 volt peak test without indication of destructive breakdown.

3.5 EVALUATION OF TEST DATA VERSUS DESIGN GOALS

The material in this section covers the comparison between results achieved and the goals set for the program with regard to capacitors. The extent by which goals were exceeded, and the extent by which goals were missed are both indicated. Further discussion of the factors involved is given in Section 4.2.

3.5.1 Capacitors

The preparation of capacitors having a capacitance of 60,000 picofarads per square inch was successfully completed. Substrates 66B05 and 66C04 are examples covering the desired range of capacitance. Other samples having capacitance as high as 2,000,000 pf/in^2 were prepared. Because of the inherent dielectric strength limitation of the material used, these very high value capacitors did not approach desired voltage characteristics.

3.5.2 Temperature Coefficient

The devices tested for temperature coefficient on substrate 66C04 exceeded the goal of 300 ppm per ^{o}C. These devices had TCC values of the order of 260 to 270 ppm per ^{o}C. Some other devices tested (on different substrates) had TCC values as high as 900 ppm per ^{o}C.

3.5.3 Stability

The temperature stability goal of +2 to 3% was not met. The best samples showed a reduction in capacitance of about 4.5% after 100 hours at 145^{o}C. The average change on substrate 66C04 was a reduction of 5% in capacitance. Dissipation factor changed favorably during aging, reducing to about one-half of its initial value.

3.5.4 Working Voltage

By the criterion of the capacitor being able to withstand a sustained application of d-c voltage, the design goal of 50 volts was met by a large number of the devices. If the criterion taken is that working voltage is one-half the voltage at which non-ohmic conduction processes begin to occur, the 50 volt goal was not achieved. For example, several devices on substrate 66B06 (45,000 pf/in^2) remained intact after extensive leakage measurements up to 100 volts D.C., and the devices on 66C03 were capable of withstanding a stress of 50 volts for an extended period of time, but no devices tested remained completely ohmic to the 100 volt level.

3.5.5 Breakdown Voltage

The design goal of a breakdown voltage of 100 volts D.C. for a capacitor of 60,000 pf/in^2 was met by the pulse 100 volt D.C. test. However, no capacitors of this value were fabrication which proved capable of reaching a stress of 100 volts without the onset of non-ohmic conduction processes. Many devices of the order to 45,000 pf/in^2 which would survive 100 volt stressing during leakage tests were prepared. Also, samples such as 66C04 and 66B05 were capable of withstanding various forms of short term 100 volt stressing.

3.5.6 Adjustment

Selective etch back of top capacitor electrodes to adjust capacitor samples to a spread of less than $\pm$ 1% is exceedingly laborious. This method of post-adjustment of capacitors is not recommended for a production technique, but can be done on a laboratory basis.

3.5.7. Nominal Value

The design goal of deposition to a specified value (60,000 pf/in^2) $\pm$10% was met. A specific example is substrate 66C04 which ranged from 56,500 pf/in^2 to 61,700 pf/^{2} as deposited.

3.5.8 Figure of Merit

The design goal was a figure of merit of 6×10^{-6} V-f/in^2. Interpretation of the achievement of this goal is subject to the particular breakdown voltage criterion applied. On the basis of a device surviving a given voltage stressing of short duration, and having a given capacitance, where the product of voltage and capacitance is in excess of 6×10^{-6}, this was met by 66C03-1 with a figure of merit of 6.05×10^{-6} V-F/in^2. On a basis of the onset of non-ohmic conduction, the best values are of the order of 3×10^{-6} V-f/in^2.

TABLE VII

Capacitance and Dissipation Factor

Sample Number		Pf/device ($9mm^2$)	Dissipation Factor	Pf/in^2
66B01	1*	shorted		
	2	900	0.46	63,400
	3	820	0.33	58,600
	4	shorted		
	5	800	0.24	57,200
	6	800	0.20	57,200
66B02	1	shorted		
	2	shorted		
	3	shorted		
	4	shorted		
	5	shorted		
	6	shorted		
66B03	1	shorted		
	2	shorted		
	3	shorted		
	4	shorted		
	5	shorted		
	6	shorted		
66B04	1	shorted		
	2	15,000	1.01	1,700,000
	3	4,000	1.0	286,000
	4	1,300	0.14	930,000
	5	10,000	1.0	715,000
	6	500	0.19	35,800

* Six capacitors per substrate.

Table VII cont.

Sample Number		Pf/device ($9mm^2$)	Dissipation Factor	Pf/in^2
66B05	1	997	0.15	70,800
	2	987	0.14	70,100
	3	930	0.08	66,000
	4	930	0.08	66,000
	5	940	0.08	66,600
	6	947	0.08	67,200
66B06	1	lead open		
	2	630	0.11	45,000
	3	shorted		
	4	lead open		
	5	630	0.11	45,000
	6	shorted		
66B07	1	635	0.05	44,700
	2	605	0.05	43,200
	3	503	0.06	42,500
	4	589	0.05	42,100
	5	603	0.05	43,100
	6	617	0.05	44,100
66B08	1	301	0.08	21,600
	2	551	0.08	39,500
	3	545	0.08	39,000
	4	520	0.08	37,200
	5	547	0.08	39,200
	6	557	0.08	39,900
66B09	1	567	0.07	40,600
	2	556	0.07	39,800
	3	558	0.07	40,000
	4	547	0.07	39,200
	5	548	0.07	39,200
	6	560	0.07	40,000

Table VII cont.

Sample Number		Pf/device ($9mm^2$)	Dissipation Factor	Pf/in^2
66B10	1	604	0.07	43,100
	2	589	0.07	42,100
	3	580	0.07	41,500
	4	576	0.07	41,300
	5	580	0.07	41,500
	6	597	0.07	42,700
66C01	1	shorted		
	2	3,275	0.005	234,000
	3	3,100	0.004	222,000
	4	2,980	0. 06	214,000
	5	3,140	0.006	224,000
	6	3,040	0.005	217,000
66C02	1	shorted		
	2	shorted		
	3	shorted		
	4	shorted		
	5	shorted		
	6	shorted		
66C03	1	1,630	0.005	116,500
	2	1,690	0.0 04	121,000
	3	1,620	0.005	116,000
	4	1,550	0.005	111,000
	5	1,610	0.005	115,000
	6	1,580	0.005	113,000
66C04	1	810	0.09	58,000
	2	825	0.06	59,000
	3	790	0.0 6	56,500
	4	833	0.06	59,500
	5	864	0.06	61,700
	6	836	0.08	59,800

Table VII cont.

Sample Number		Pf/device ($9mm^2$)	Dissipation Factor	Pf/in^2
66C05	1	shorted		
	2	7,320	0.02	524,000
	3	shorted		
	4	shorted		
	5	7,810	0.02	559,000
	6	7,600	0.02	544,000
66C06	1	3,500	0.04	245,000
	2	3,680	0.04	263,000
	3	3,620	0.04	259,000
	4	3,800	0.07	272,000
	5	3,840	0.06	274,000
	6	3,550	0.06	254,000
66C07	1	30,000	0.63	2,140,000
	2	40,000	0.76	2,860,000
	3	37,000	0.68	2,640,000
	4	34,000	0.67	2,430,000
	5	33,000	0.67	2,360,000
	6	28,000	0.70	2,000,000

TABLE VIII

Temperature Coefficient of Capacitance

Sample Number		Temperature Change(°C)	Capacitance Change (Pf)	TCC(PPM/°C)
66C04	5*	75**	17.2	262
	6	75	17.2	271

* Six capacitors per substrate.

** 25°C to 100°C.

TABLE IX

Breakdown Voltage
Onset of any Non-Ohmic Conduction
Uncertainty Band (Volts)

Sample Number		Bottom	Top
66C04	1 *	47 volts	60 volts
	2	38	48
	4	30	30
	5	35	45

* Six capacitors per substrate.

4.0 ANALYSIS OF TEST DATA

The test data gained during the course of this program has indicated the nature of a number of basic phenomona. The discussion of these indications has been compiled in Section 4.1 and 4.2. These sections cover the aspects of resistor fabrication and capacitor fabrication respectively.

4.1 RESISTORS

During the course of this program, three major areas of relationship with regard to resistor properties have been isolated. These are composition (specifically with regard to oxygen content of a metal film), structure of the resistive film and geometry of the film (primarily in terms of thickness). The relationships involved give some indication of the ultimate parameter limits which can be reached in the fabrication of metallic thin film resistors.

4.1.1 Composition and Properties

When high resistance devices were being fabricated and tested, a relationship between the factor of residual oxygen and moisture in the system and thermal noise of the resistors was noted. Steps were taken to control and measure these residuals, with a subsequent reduction in the noise of high value resistors. The present hypothesis is that oxygen inclusion in the resistive films forms barriers through which conduction occurs by non-ohmic processes. The processes involved also contribute to the negative TCR. These non-ohmic processes are of a statistical nature, giving rise to random conduction bursts. This means that any sample with a large oxygen inclusion content will be noisy. The hypothesis definitely checks against experimental data with regard to noise.

4.1.2 Structure and Properties

It has been hypothesized that the cold substrate deposition process forms films which are continuous at very small thicknesses. The

island structure of thin films formed by conventional deposition techniques has been suggested as a basis for noise and negative temperature coefficients of resistance. A dependence of TCR on point defects in the metal films has also been hypothesized. This is cited by R. E. Thun, et al, on page 183 of Microelectronics, Theory Design and Fabrication (edited by Edward Keonjian, McGraw-Hill, N. Y., 1963). It appears that cold substrate deposition can be used to achieve optimum structure for resistors and thereby extend the useful range of resistances.

4.1.3 Geometry and Properties

Metallic resistive films, having thickness of the order of one electron mean free path, exhibit properties considerably different from those of the bulk metals. The cold substrate deposition process does not have an effect upon this, except in the case of structure-sensitive parameters. The very thin films are normally quite structurally sensitive, however, and it appears that the cold substrate process forms films which are more stable than conventionally deposited films.

4.1.4 Ultimate Limits

The ultimate limits of sheet resistance of thin film resistors which have satisfactory operating parameters appear to be on the order of 10^5 ohms per square. This limit depends on the development of techniques which avoid the possibilities of island formation, oxygen inclusion, and environmental modification of structure. With such techniques, it should be possible to form resistors having TCR values of the order of 100 PPM/^{o}C, current noise of the order of -25 db to an index of one microvolt per volt, and which are stable over long operating times under environmental conditions. This will require that the resistors are, in effect, sealed as they are formed and that a high degree of control is exercised on the formation environment. There should be no difficulty in preparing such resistors to a $\pm$ 1% tolerance without trimming.

4.2 CAPACITORS

Major relationships between the properties of capacitors and the three parameters (composition, structure and geometry) for the dielectric layer are apparent. These parameters control the quality and the figure of merit of capacitors.

4.2.1 Dielectric Composition and Properties

The dielectric layer material used in this program was silicon monoxide. From some aspects, this is an excellent material to work with. From others, it is one of the poorer materials. SiO has a fair dielectric strength (of the order of 2×10^6 V/cm), and a good dielectric constant for example, 5. However, the dielectric constant is highly sensitive to the state of oxidation of the silicon and may range from about 4 to about 8. Moisture sensitivity of silicon oxide dielectrics is also somewhat a function of composition. These factors mean that the system pressure, residual gas composition, deposition rate, and source temperature must be controlled closely in order to produce thin film capacitors repeatedly from SiO. A precisely repeatable deposition cycle with SiO will give a good yield of capacitors, but the cycle must be precise.

If a larger product of dielectric constant and dielectric strength is desired - as might be dictated by the design voltages and capacitances per unit area for certain applications - materials other than SiO should be considered. There are other oxide systems, having desirable stability properties, which should produce a figure of merit at least twice that attainable by the use of silicon monoxide. An example is a mixed oxide of dysprosium, boron, and silicon. Systems such as this offer high capacitance, high working voltage, high temperature operation, and low temperature coefficient if they are properly formulated. They also present unique problems of fabrication.

4.2.2 Dielectric Structure and Properties

The optimum dielectric layer for capacitor use is an extremely dense

one. Gross defects such as pinholing obviously can cause shorting. Other forms of defects can also degrade the dielectric; for example, lattice vacancies could contribute to tunneling and field ionization phenomena, both undesirable in the case of capacitors. This does not mean that, on the ultimate level, one needs or wants a single crystal dielectric. Silicon dioxide is an excellent example of a material which has a higher dielectric strength in the amorphous form than it has in the crystalline form. The point here is that the ideal dielectric has no voids, and is in the closest possible packing for its structure.

4.2.3 Dielectric Geometry and Properties

The noraml capacitance formula applies to film capacitors. There are some slight deviations as the dielectric films are made very thin. One of these is an increase in dielectric strength if the very thin film is nearly perfect. This increase is due primarily to short range phenomena. Uniformity of dielectric thin films is usually better on a percentage basis if they are fairly thick. This means that there will be less opportunity for local breakdown in a thick dielectric layer. In order to have both high capacitance and a thick layer, a high dielectric constant material is needed. This returns the problem to the materials area.

4.2.4. Ultimate Limit s

The ultimate limits for thin film capacitors using silicon monoxide dielectric layers lie somewhere in the vicinity of a hypothetical capacitor having composite best parameters as obtained under this contract. The figure of merit limit is of the order of 6×10^{-6} V-f/in^2 for 100 volt breakdown capacitors, which places the maximum capacitance at about 60,000 pf/in^2. To achieve higher values, for example, a figure of merit of the order of 13×10^{-6} V-f/in^2 , other material systems must be considered. The materials system, which will give

such a figure of merit while retaining a low temperature coefficient of capacitance, very likely will be a mixed oxide system with one component being of the rare earth family. There is evidence that such systems will be operable at temperatures well in excess of the operating temperature of present day active devices of the solid state form.

5.0 RECOMMENDATIONS AND CONCLUSIONS

This program has shown that resistors, with high sheet resistance and having other desirable characteristics, can be deposited in sets which have a spread of less than plus or minus one percent, by means of cold substrate deposition. It has also shown that high capacitance, low leakage capacitors, having useful working voltages, can be prepared by the same means.

This is only the first step toward the application of cold substrate deposition to problems of fabrication of microcircuit systems. In order that the potential advantages of this process may be seen, it is helpful to provide additional comments about the process, per se.

The process can be conducted in such a manner that tenacious bonding between evaporant and substrate can be achieved at room ambient substrate temperatures for materials which, by conventional means, must be deposited at substrate temperatures of 150°C to 400°C in order to ensure adhesion. This inherent feature led to the naming of the process. Such a feature is attractive, for example, when using ordinary photoresists for rejection masking. In the case of cold substrate deposition, adhesion of the deposited films is dependent on chemical bonding. A weak link of a thin film system may be the lack of either adhesion of one layer to another or cohesion within a single layer. In either case, for the cold substrate deposition process, the limiting factor is the strength of the chemical bonding involved. This may be metallic bonding, covalent bonding, ionic bonding, or any form of intermediate bonding.

Other benefits inherent in this process include the ability to form very thin films of high integrity and to provide some control of the structure of the deposited layer.

With the preceding comments on the cold substrate process in mind, it becomes possible to formulate logical areas of study which will lead to the successful solution of problems in microcircuit technology.

5.1 RESISTORS

The areas to be further studied with regard to resistors are the high-value, small-area devices for hybrid and monolithic circuitry. Most factors of technology for this type of device can be interchanged directly between silicon monolithic and glass/ceramic substrates. Because of the more severe "real estate" problem with monolithics, the recommended course is the application of cold substrate deposition to the fabrication of resistors for silicon integrated circuits. This will provide a range of resistors having properties presently not available for monolithic circuit design. The combination of close tolerances, low TCR, and high sheet resistance makes this area of attack very attractive.

5.2 CAPACITORS

The present state of the art for capacitors prepared by cold substrate deposition is near the theroretical limits for silicon monoxide dielectric. The next stage of development will be to utilize other dielectric materials. It appears advantageous to do this for silicon integrated circuits for the same reasons that apply to further development of resistors.

5.3 ACTIVE CIRCUIT ELEMENTS

The extreme versatility of the cold substrate deposition process, particularly in the areas of forming films of highly refractory materials, and in forming films of compounds and alloys of specific properties, leads to the potential goal of thin film active elements by this method. In order to extend the application of the cold substrate process to the fabrication of complete electronic circuitry, additional studies will have to be performed, relative to the structural and electrical properties of the film.

The ultimate purpose of these studies would be to develop, optimize and control the deposition parameters of the cold substrate process to provide films of active-device qualities. As all types of active devices are both structure as well as surface sensitive, the evaluation program of the films should include:

1. Determination of degree of crystallinity and crystal perfection by X-ray diffraction and electron microscopy.

2. Determination of film resistivity, carrier mobility and surface state density by means of Hall measurements.

5.4 HYBRID CIRCUIT APPLICATIONS

The cold substrate process has great potential for use in hybrid circuits for both passive component fabrication, as discussed earlier, and conductor deposition for interconnection. As an example, the cold substrate process provides a means of forming diffusion and migration barriers to prevent undesired alloy formation and reaction. Application of such barriers is cited in the following interconnection problem. The lowering of adhesion of contact pad structure can be prevented by introducing a barrier to tin and lead diffusion (for example, nickel), which is covered by a solderable metal (for example, gold). With cold substrate deposition, it is even possible to build a solder preform into a contact pad and protect it from oxidation. For example, an aluminum-nickel structure can be given a flash of gold, a heavy deposit of tin-lead solder, and a final gold flash. Such a structure, placed in intimate contact with a similar structure and heated, would need no fluxing. Solder alloys are naturally not limited to the tin-lead system.

In a similar manner weldable structures can be prepared by applying a suitable sheathing material after deposition of a low resistance material. One system which has been studied to some degree is that of titanium-copper-nickel.

5.5 MONOLITHIC CIRCUIT APPLICATIONS

The application of cold substrate deposition to conventional monolithic microcircuit fabrication is attractive from the standpoints of potentially

greater reliability and low cost. These benefits stem from several factors. The first of these is the proposed elimination of the alloying step in forming aluminum-silicon contacts, thus removing a critical high temperature cycling process. The second is that dielectric films can be prepared under low temperature conditions, thereby removing subsequent high temperature cycling steps, and eliminating a shear and bending stress situation which is inherent in thermally grown SiO_2 films on silicon. A third is that the cold substrate deposition process can be used to form high resistance precision resistors. This provides a means of reducing the substrate area devoted to such resistors.

The potential cost saving for conventional monolithic microcircuit fabrication would come about due to the shorter process time and improved yield.

5.6 THIN FILM CIRCUIT APPLICATIONS

The development of an active thin film device by cold substrate deposition will lead to a total thin film circuit capability. The probable type of such a device is the thin film field effect transistor. This, in conjunction with the technology discussed under the heading of Hybrid Circuit Applications, gives a total thin film circuit capability with extremely desirable characteristics.

Appendix I

DESIGN GOALS

Utilizing a cold-substrate deposition process, produce resistors having the following minimum design goal requirements:

(a) Sheet resistance 10^2, 10^3, 10^4, and 10^5 ohms per square.

(b) Temperature coefficient of resistance (T.C.R.) $\leq$ 100 ppm/^{o}C for resistors in the range 10^2 - 10^4 ohms/square. The T.C.R. of 10^5 ohms per square material will be measured but no extensive effort will be made to achieve 100 ppm/^{o}C.

(c) Operating temperature range, -30 to 145^{o}C.

(d) Adjustment $\pm$ 1%.

(e) Current noise db -35; μ v/v in a decade as recommended by NBS.

(f) Nominal value without adjustment $\pm$ 10%.

(g) Stability $\pm$ 1 to 2%.

(h) Moisture-humidity effects $\pm$ 1%.

Utilizing a cold-substrate deposition process, fabricate capacitors having the following minimum design goal requirements:

(a)	Capacitance	$\geq$ 60, 000 pf/in^2
(b)	Temperature coefficient	$\geq$300 ppm/^{o}C
(c)	Stability	$\pm$ 2 to 3%
(d)	Working voltage	$\geq$ 50 vdc
(e)	Breakdown voltage	$\geq$ 100 vdc
(f)	Adjustment	$\pm$ 1%
(g)	Nominal value without adjustment	$\pm$ 10%
(h)	Figure of merit	6 X 10^{-6} v-f/in^2

Appendix II

Specimens Meeting Design Goals

Resistors

	Design Goal	10^2 ohms/sq.	10^3 ohms/sq.	10^4 ohms/sq.	10^5 ohms/sq.
(a)	Sheet Resistance	66A16 66A29	66A17 66A23	66A57 66A75	66A55
(b)	Temperature Coefficient of Resistance	66A16 (3 devices* <100 ppm 4th @ 103 ppm) 66A20 (all devices)	66A17 (3 devices)*	Best value: one device on 66A41 was 476 ppm.	Comparable to values for 10^4 ohms/sq.
(c)	Operating Temperature	66A16 66A14 66A29	66A17	66A68	66A54
(d)	Adjustment	66A12 adjusted to ±0.12%	(This applies as well to the other resistance ranges, since the adjustment technique merely involved altering the geometry).		
(e)	Current Noise	66A16 66A20 66A14	66A17 66A46	Best value: one device* 66A75(1) -24.5 db.	Not met.

* "Devices" refer to industrial resistors on a substrate containing four resistors.

Appendix II (cont'd)

Resistors

	Design Goal	10^2 ohms/sq.	10^3 ohms/sq.	10^4 ohms/sq.	10^5 ohms/sq.
(f)	Nominal Value ±10%	66A16	66A17	66A45 (3 devices)*	66A55 (3 devices, one device was 10.1%).
		66A29	66A23	66A57 (3 devices)*	
				66A75 (3 devices)*	
(g)	Stability	66A14	66A17	Not met.	Not met.
		66A05			
(h)	Moisture Humidity Effects	0411C	66A49	66A41 (1 device)*	66A52 (2 devices)*
		66A48			

Appendix II (cont'd)

Specimens Meeting Design Goals

Capacitors

		Sample No.
(a)	Capacitance	66C04 66B05
(b)	Temperature Coefficient of Capacitance	66C04
(c)	Stability	Not met.
(d)	Working Voltage	66B06 66C03
(e)	Breakdown Voltage**	66C04) Short term 66B05) 100 volt stressing.
(f)	Adjustment	66C07
(g)	Nominal Value without Adjustment	66C04
(h)	Figure of Merit	66C03

** Based on short term 100 volt stressing.

Appendix III

TECHNIQUE FOR PHOTOMASKING ON LIGHT SCATTERING SUBSTRATE MATERIALS*

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It is desirable in some thin-film device fabrications to use photomasking techniques on the first surface of a dielectric substrate. In this approach, a coat of photoresist, applied directly to the substrate surface, is exposed to radiation through a photographic mask. This fabrication method is used, for example, when the substrate itself is to be etched, or when the photoresist serves as a rejection mask for a subsequently deposited film. In others, it may be desirable to photoetch a transparent layer on the first surface of the substrate. Many of the more useful dielectric substrate materials are transparent to ultraviolet radiation of the wavelengths to which photoresist materials are sensitive. This fact complicates the photomasking, in that any ultraviolet passing through the photoresist layer during exposure can be reflected back under the edges of the exposure mask to wash out the edge of the resist pattern. This communication offers a solution for this problem.

Two types of substrate are normally encountered. These are the transparent substrate such as clear quartz or sapphire and the scattering substrate such as 99 percent alumina, which is translucent. These two types of substrates present light reflection problems (which require different approaches for solution).

The transparent substrate material reflects light from the second surface (Figure 1). This detrimental effect on image edge definition can be minimized by using a light-absorbing coating on the second surface. The material used should have an index of refraction which matches fairly well with that of the substrate to minimize interface reflection. This technique is fairly standard. For most applications, one of the best coating materials is 3M velvet coating optical black, which is available in several forms. [1]

The scattering substrate not only reflects light from the second surface, but also creates internal light scattering (Figure 2). This latter effect cannot be corrected by introducing a second surface coating. It has been found that a precoating of the first surface of the substrate with a material such as silicon monoxide will prevent image washout on scattering substrates. A coating of SiO, between 5,000 and 10,000 angstroms thick, performs satisfactorily (Figure 3). The major optical requirement is that the coating should be highly absorbent to wavelengths shorter than 500 millimicrons. This means that the technique is not necessarily limited to SiO as an ultraviolet blocking layer.

The technique described here has been successfully used to produce sharp photomask images on ceramic substrate materials, upon which only poor quality images could be produced by other methods.

Acknowledgment

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References

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(1) 3M Reflective Products Division, Minnesota Mining and Manufacturing Co., General Offices: 2501 Hudson Road, St. Paul 19, Minnesota.

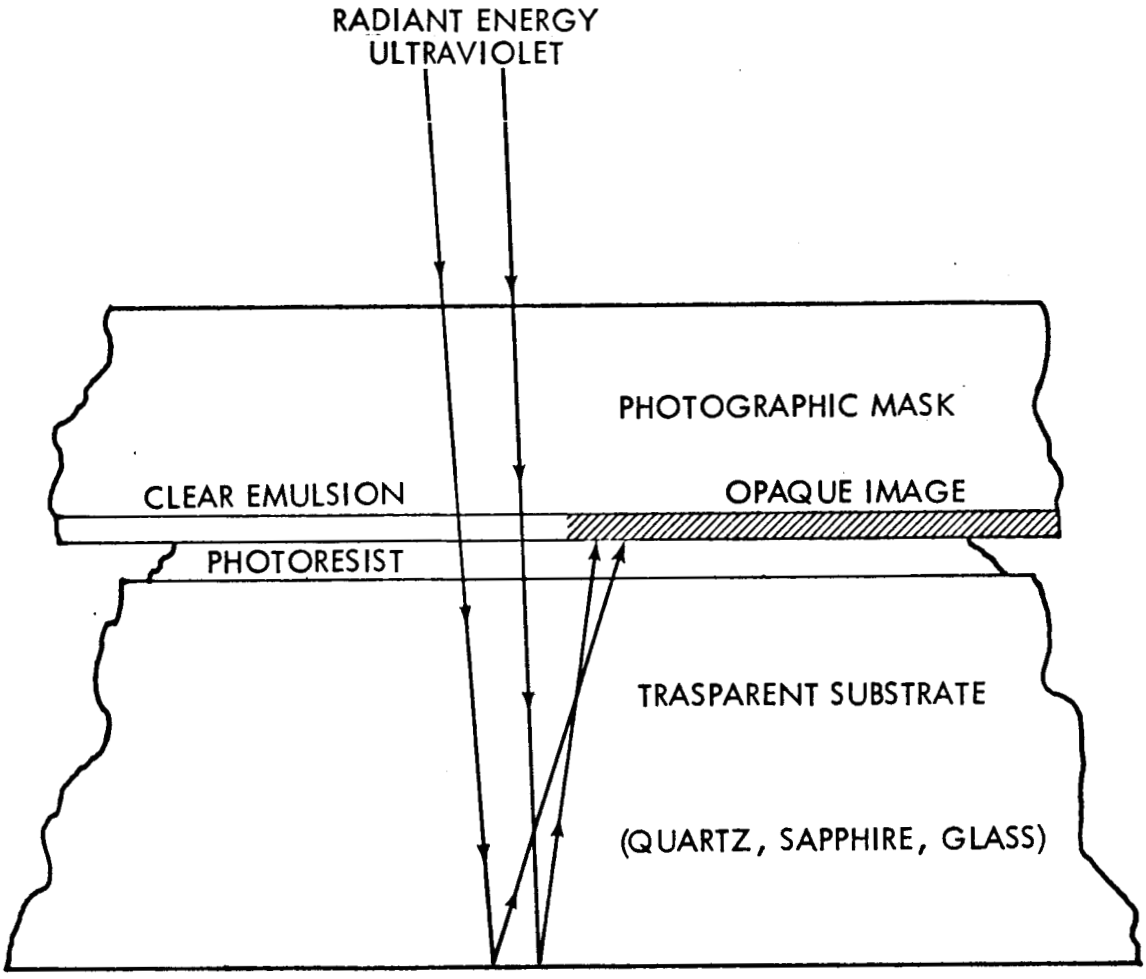

Figure 1. Image Decay by Second Surface Reflection of Transparent Substrate Material

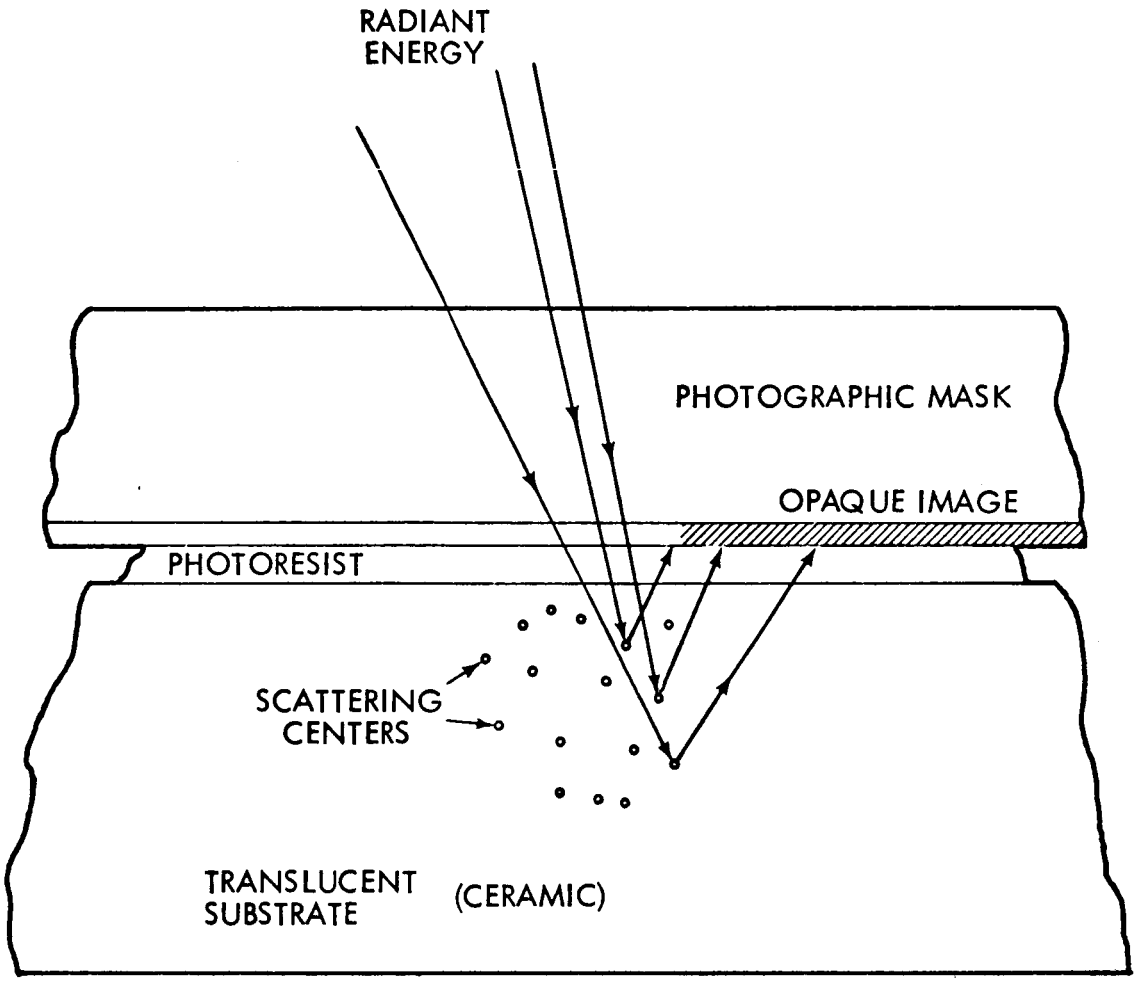

Figure 2. Image Decay by Internal Reflection of Translucent substrate Material

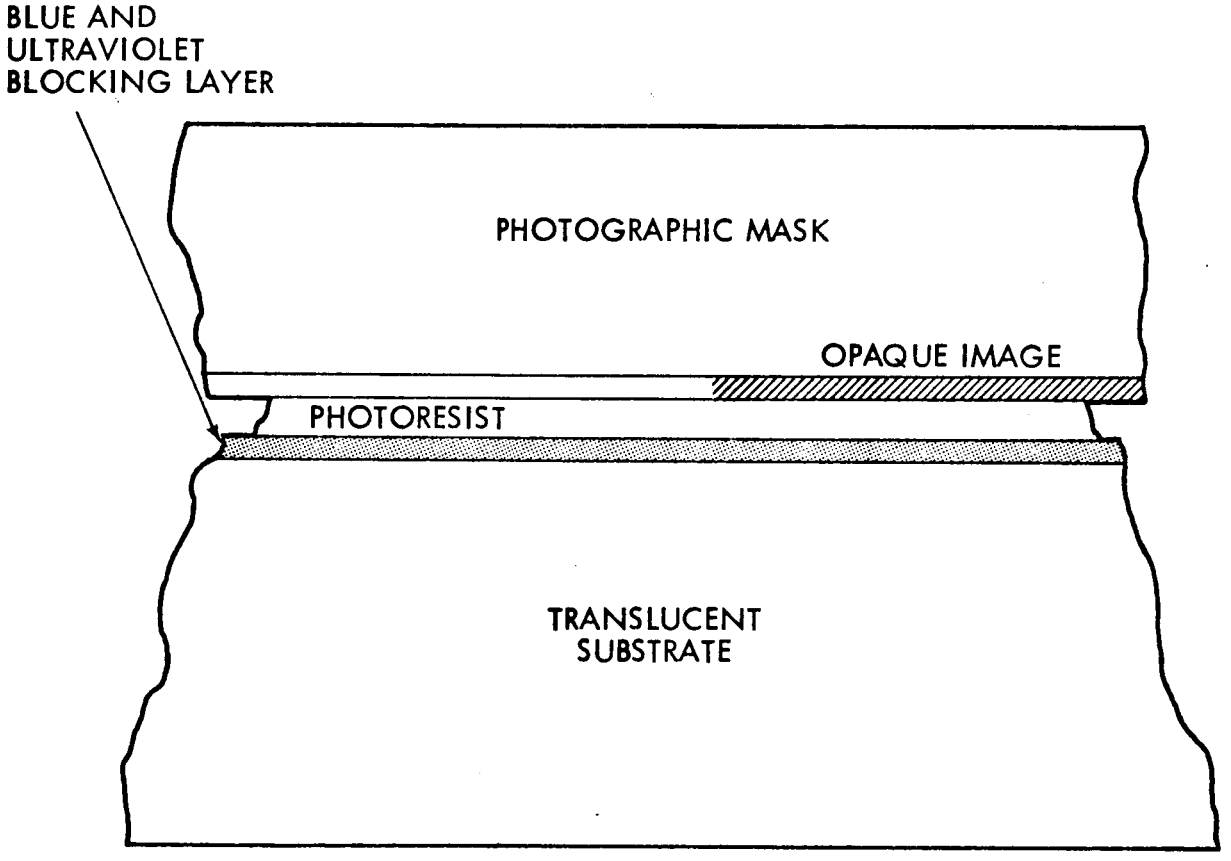

Figure 3. Interposition of an Ultraviolet Blocking Layer on Translucent Substrate